FPGAS TAKING OVER THE ASIC MARKET IS A MYTH

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Max, Max, Max – Now you know I believe that most SoC designs will be done in FPGAs and nothing I say here is meant to deny that fact; however your promotion of the myth that **FPGAs are driving the ASIC vendors** from the battle field is ridiculous. First of all I recommend you contact Bryan Lewis at Gartner-Dataquest. He's been producing his Design Start report for well over 15 years now and it is considered the bible in this area.

Let's look your statement that "FPGAs can now play in applications and markets that were previously owned by ASICs". Your assumption seems to be that technically these designs are stagnant. Now I'm sure that an FPGA can be used in the design of a cell phone, circa 1998, but things have changed a bit. As FPGAs are reaching tens of millions of gates, ASICs are now shooting for a billion gates. As the functionality increases so does the ASIC gate counts.

The biggest surprise in my recent Design Seat Count report was the 10% decline in FPGA seats during the Great Recession. It turned out that the recession wasn't the main cause of the decline. I remember being on a panel with Wes Paterson, when he was VP of Marketing for Xilinx. We were discussing the difference between FPGA gates (or Paterson Gates as we fondly called them) and ASIC gates. Wes made the statement that the main difference was that you didn't need to simulate an FPGA gate. Well the days of Blow and Go designing are Blown and Gone. Now designing an FPGA SoC is just as challenging as designing an ASIC SoC. The skills of today's FPGA designer have been ratcheted up quite a few notches and this has caused us to lose design seats over the past few years. The only difference between the two designers today is the quality of their design tools and once FPGA designs start exceeding forty million gates that will have to change too.

Your good friend,
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