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Design Technology Improvements and Impact of Designer Productivity

Concurrent Software Infrastructure	A set of tools that allow concurrent software development and debug
Executable Specification	A design flow that has no manual processes from the specification to completed system and that can be completely validated at each step
Heterogeneous Parallel Processing	Parallel Processing using different application specific processors for each of the separate functions in the system
Homogeneous Parallel Processing	Many identical processor cores which allow for performance, power efficiency and high reuse (SMP)
IC Implementation Tool Suite	Tightly integrated tool set that goes from RTL Synthesis to GDS II through IC Place and Route
In-House Place and Route	The transfer of the IC Place and Route function from the semiconductor vendors to the design team
Intelligent Test Bench	A verification tool (cockpit) that takes in an ES Level description and partitions it into verification blocks, then executes the proper verification tools on the blocks; while tracking and reporting coverage
Reuse – small blocks	Blocks from 2,500 – 74,999 gates
Reuse – large blocks	Blocks from 75,000 – 1M gates
RTL Functional Verification Tool Suite	Tightly integrated RTL verification tool suite including all simulators and formal tools needed to complete the verification process
System Design Automation	True System Level design including Electronic hardware and software, Mechanical, Bio, Opto, Chemical and fluids domains
Tall Thin Engineer	The presence in the Design Team of at least one senior engineer who has experience in all phases of the design process
Transactional Memory	A concurrency control mechanism analogous to database transactions for controlling access to shared memory in concurrent computing. It functions as an alternative to lock-based synchronization
Transactional Modeling	The development of standard SystemC models at the Transaction Level of abstraction
Very Large Block Reuse	Blocks that exceed 1M gates