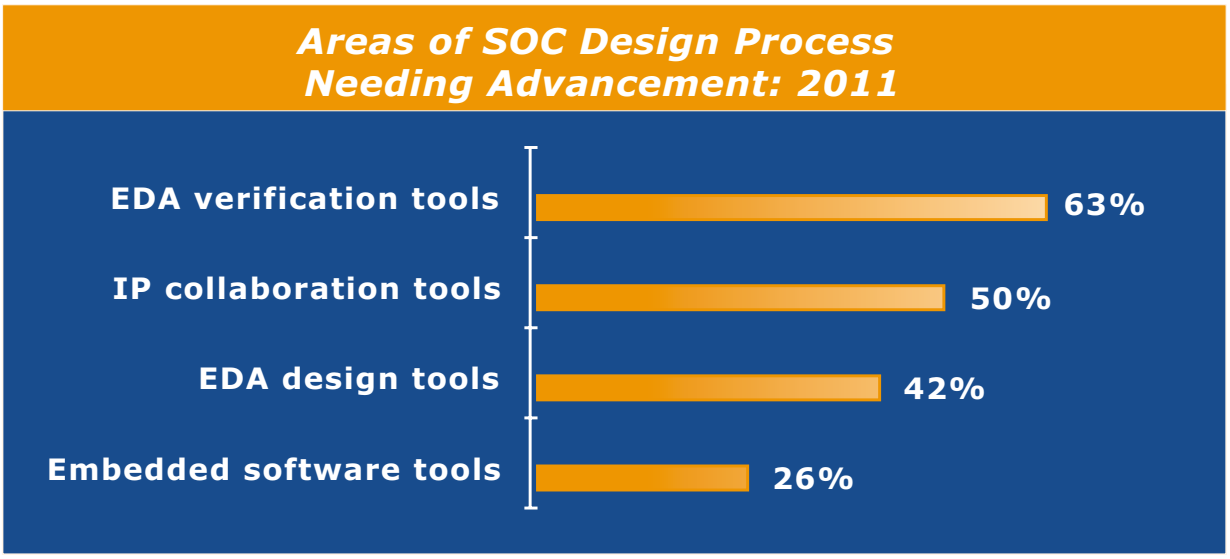
IP REUSE

The areas of SOC/IC design processes that engineers stated needed the most advancement in the next two years are shown in *Figure 1*. Based on a recent survey of 465 SoC designers and managers, the top two areas for investment were verification tools at 63 percent, and IP (intellectual property) collaboration and reuse tools at 50 percent. 42 percent selected EDA design tools.

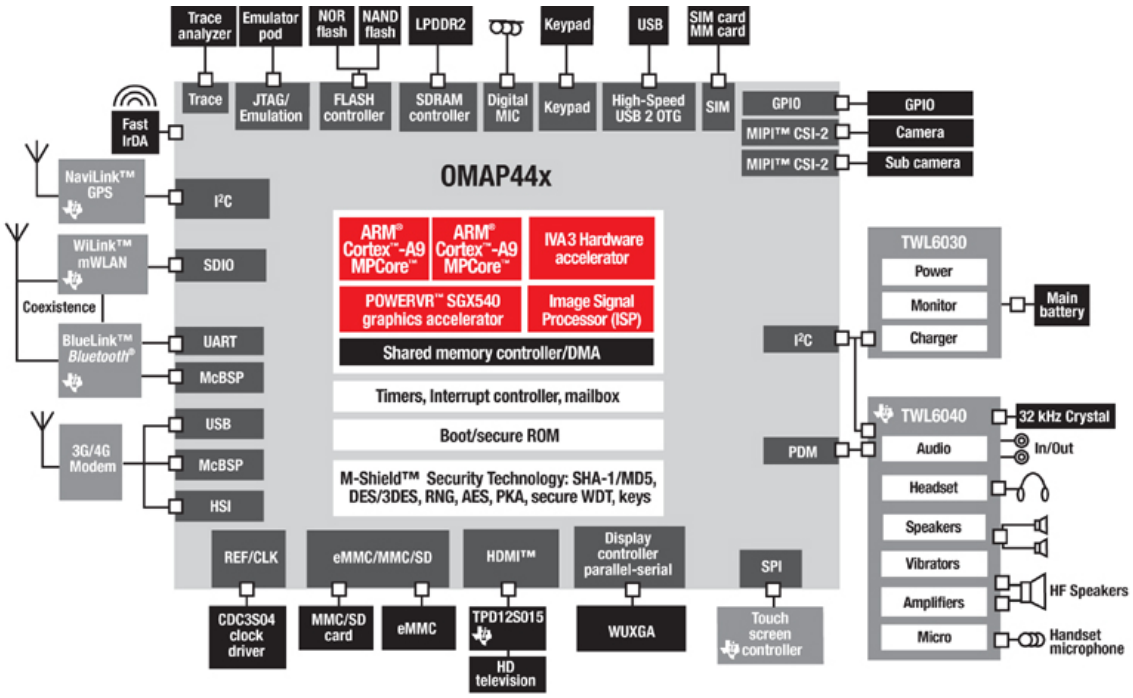
Figure 1: Managing Semiconductor IP — Top Challenge



Online survey run April 2011 by LaunchM 465 respondents.

Companies in the fastest growing segments of the electronics industry are designing-in and adopting mixed-IP based designs in 45nm and 65nm System On Chip (SOC). A 45nm 4G baseband SOC design, as shown in *Figure 2*, carries an explosion of bandwidth with up to hundreds of Mbps (Megabits per second).

Figure 2: Complex IP case: OMAP 4G Platform



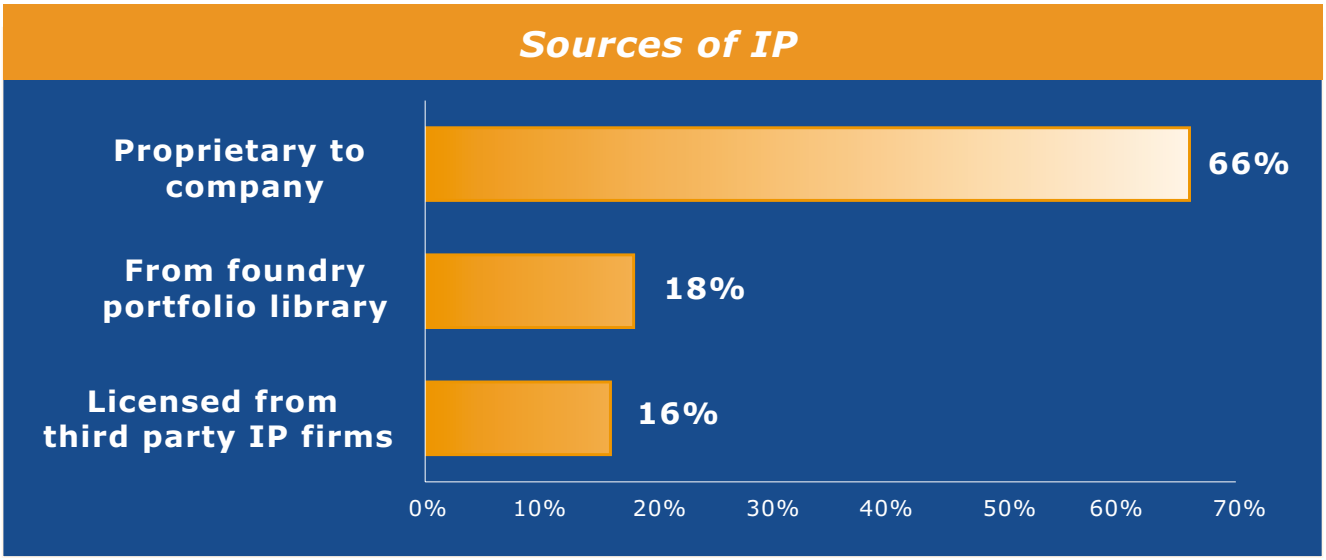
Source: Texas Instruments, 2011

At this level, the efficiency of integrating semiconductor IP becomes more important to reduce cost, shorten design cycle and reduce test time. However, as noted by Dr. Aseem Gupta of Freescale Semiconductor "IP based design is not as simple (tracking and fixing bugs), firm, organized, and safe as it sounds". As the industry gets ready to ramp up production of 45nm technology followed by 22/20nm designs for 2012, complex IC design integration will require more design data management to help reduce cost, reduce time, improve reliability and optimize the most appropriate mix and match of IP.

Semiconductor IP comes from many data sources, internal databases and file systems. GSA recently reported that 66 percent of IP is internally developed, 18 percent is from the foundry portfolio library, and 16 percent is licensed from third party IP vendors. ***(See Figure 3)***. The IP data can be incompatible with internal design flows, creating integration challenges. Identifying and fixing IP and fixing IP bugs can be unwieldy as a result of interdependencies across the IP versions, the design, and derivatives. Assembling and reusing IP is increasingly difficult due to the number of dynamically changing properties associated with each IP module.

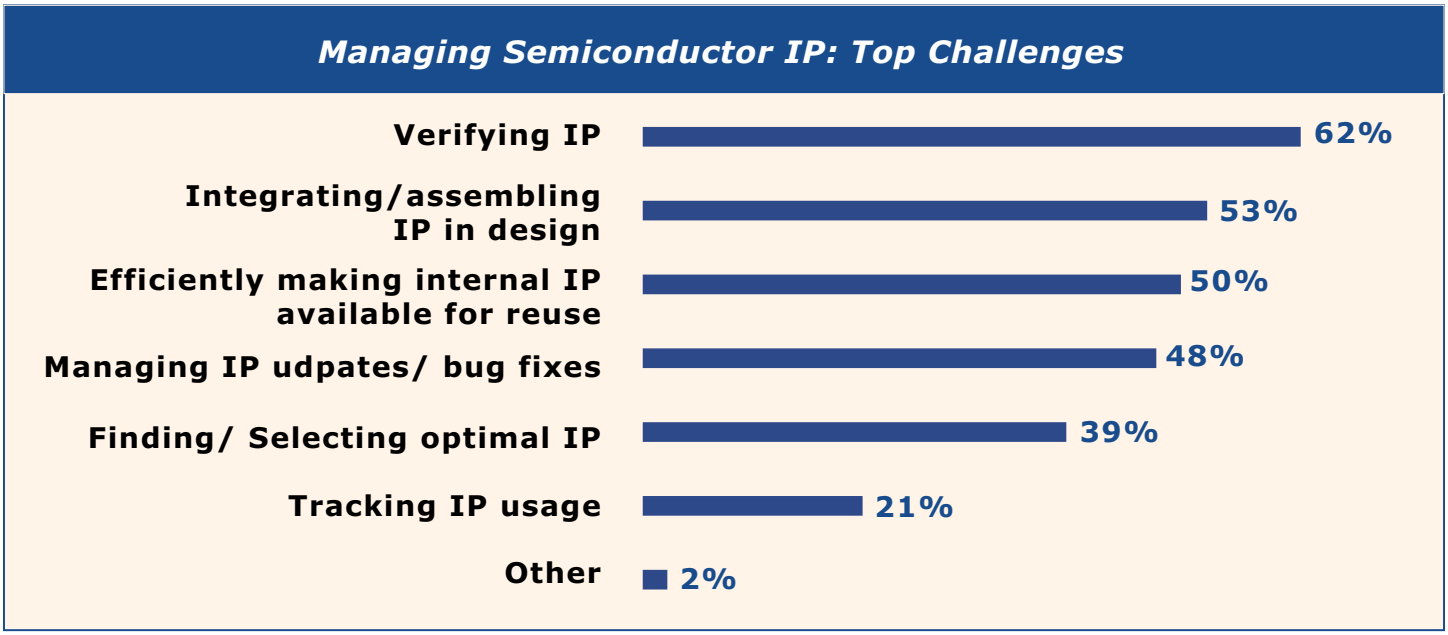
As seen in ***Figure 4***, the top challenges for managing semiconductor IP are verifying the IP, integrating and assembling the IP in the design, efficiently making internal IP available for reuse, and managing IP bug fixes and updates.

Figure 3: IP Sources



Source: 2010 Wharton-GSA Semiconductor ecosystem survey

Figure 4: Managing Semiconductor IP -- Top Challenges

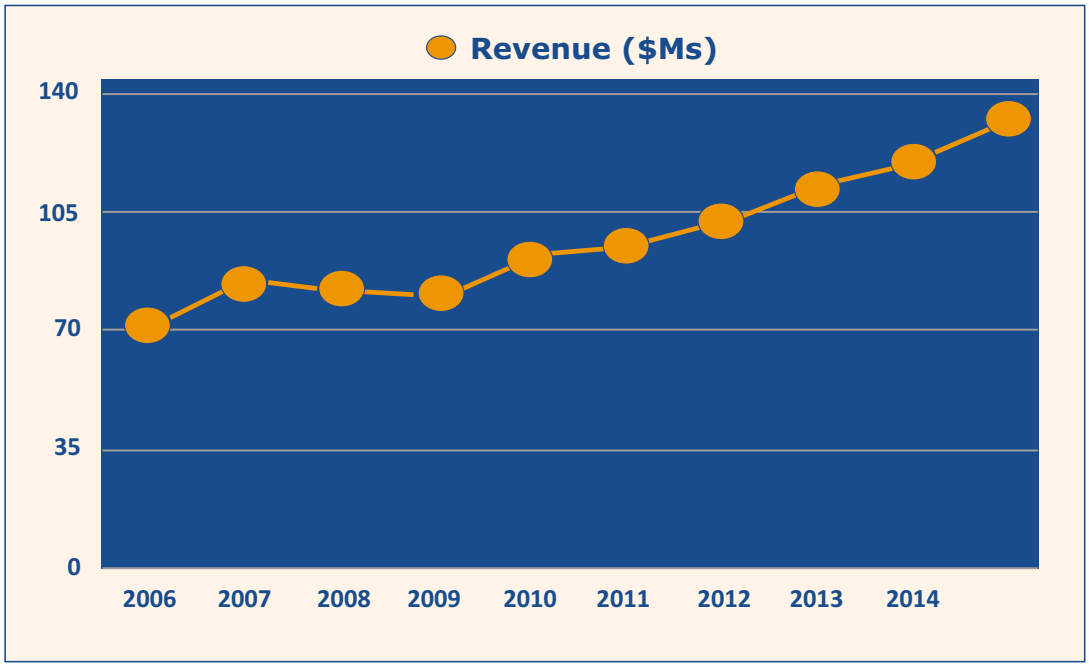


Source: LaunchM 2011 survey

FUTURE TRENDS IN IP REUSE AND SOC DESIGN

One area of growth is expected in the area of complex SOC/SIP/POP, 3D/TSV and other IP integration strategies. Gary Smith EDA expectations for SOC growth are shown in its recent forecast in ***Figure 5***.

Figure 5: Worldwide SOC Forecast



Source: Gary Smith EDA, June 2011

Beyond 2015 to 2017, companies like Apple, IBM, Intel, Qualcomm, Samsung and Texas Instruments as well as foundries will be pushing SOC and 3D/TSV designs into high-level and highly complex custom applications. They will be using multiple types of internal and third party IP solutions for four major applications such as those listed in ***Table 1***.

Table 1: Future Application Designs Driving IP Reuse

Value	Consume	Mobile	Compute/Storage	Communications
Cost	Low	Low/Medium	Medium/High	Medium/High
Volume	High	High	Medium	Medium
IP Complexity	Low	High	Medium	Medium
Gates/Trans.	<Millions	<Millions	Millions	>Millions
Devices	2D	2D/3D	2D/3D/SOC	2D/3D/SOC

DESIGN DATA MANAGEMENT

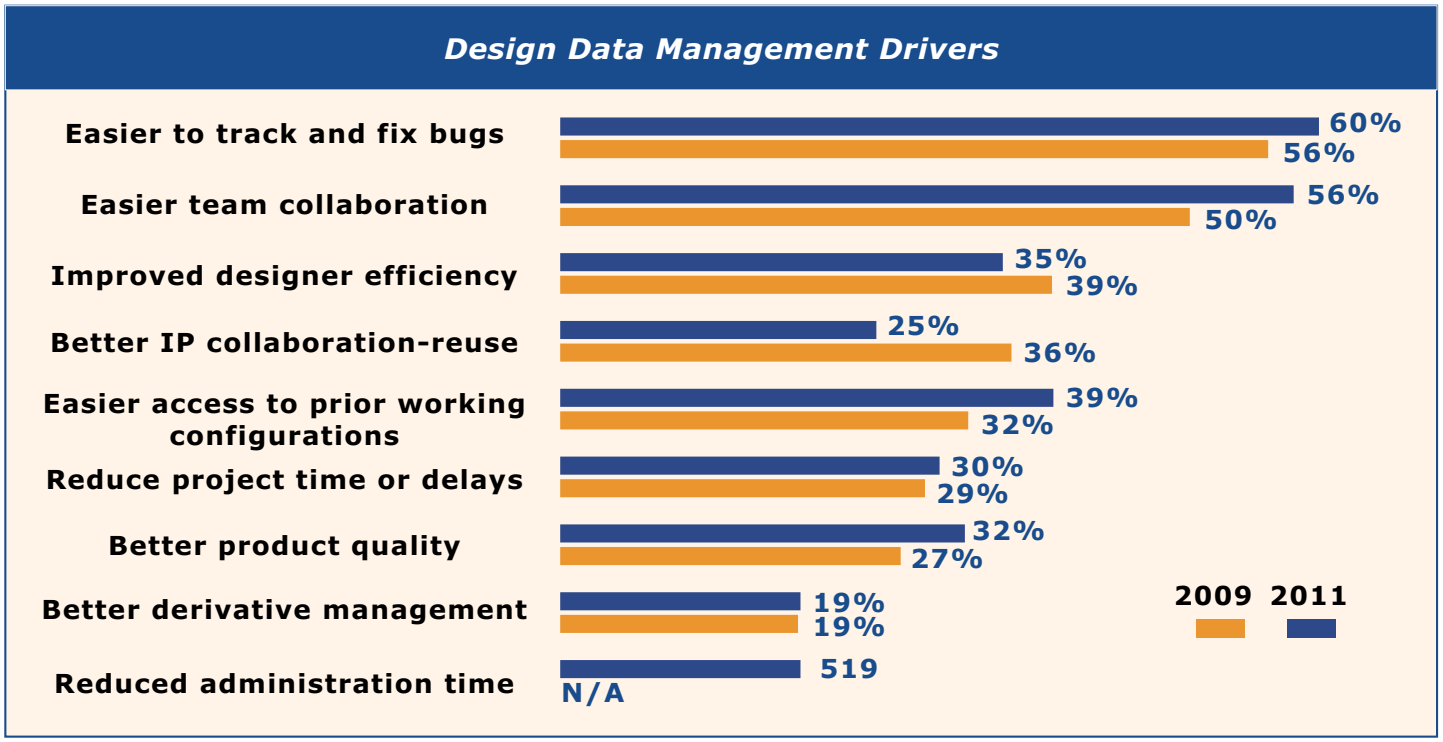
Design data management system deployment in organizations grew from 42 percent in early 2009 to 55 percent in early 2011, a cumulative growth rate of over 31 percent over the two year period. Plans to evaluate or implement design data management deployment grew from 12 percent to 21 percent over the same two year period.

Some of the primary reasons that engineers and engineering management state as to why it was becoming important to use a design management system can be seen in *Figure 6*. During the time period from 2009 and 2011, the main reasons for using design data management system tools continue to be:

- The ability of the system to accelerate the process of tracking and fixing bugs. Bugs or design failures can be a result of internal IP reuse as well as a problem with 3rd party IP reuse.
- The design management system's ability to enable efficient team collaboration (multiple teams across geographic locations) when dealing with increased design complexity.

IP Reuse's rating as a design management driver grew from 25 percent to 36 percent over the time period.

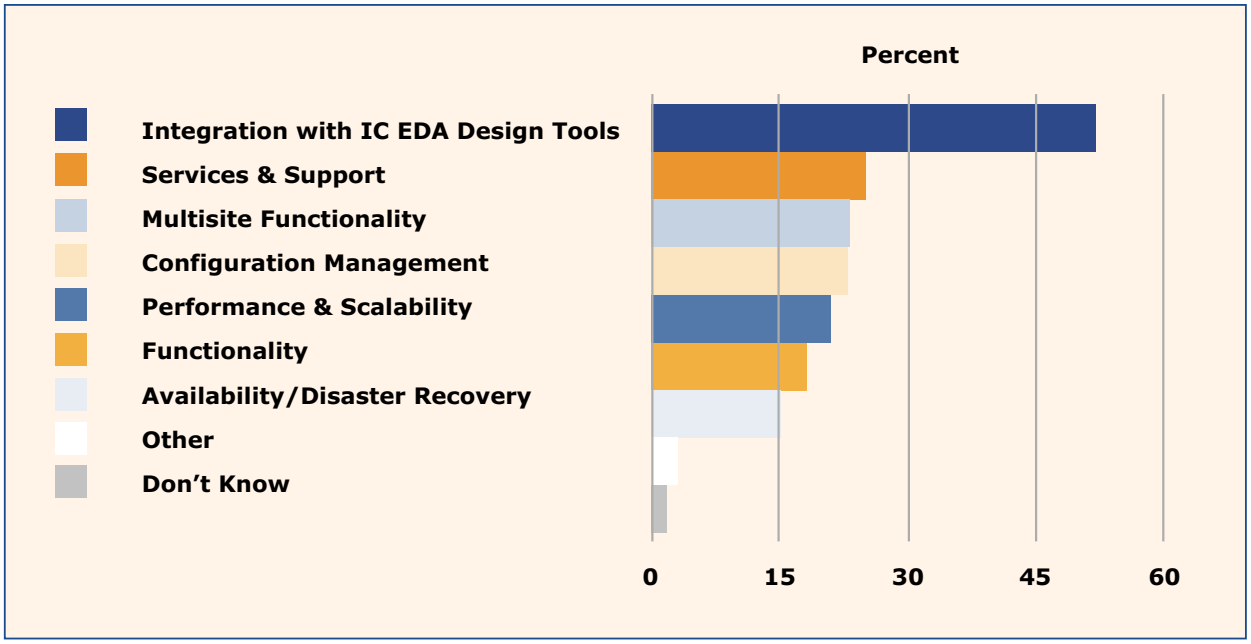
Figure 6: Design Management Drivers



Source: LaunchM 2011 survey

Today, both commercial design management and open source revision control systems are in use. Designers surveyed cited that the most important design functions missing from Open Source systems was integration with EDA tools as shown in ***Figure 7***.

Figure 7: IC Design Functions Missing from Open Source Design Management Systems



Source: LaunchM 2010 survey, 426 SoC & IC designers, engineering managers

IC MANAGE INC.

2003 was a recovery year in the electronics industry and the founding of multiple start-ups in the EDA (Electronic Design Automation) industry. One company founded during that industry up-cycle was IC Manage Inc. that focused on Design Data Management, developing its Global Design Platform (GDP) set of tools. Its suite of tools was created for use with existing full-custom, mixed-signal and digital design flows. These tools monitor the driving forces behind design data management systems and the impact on a semiconductor company's management's ability to guarantee that reliable design content is always available to all engineering design teams. As noted by Shiv Sikand, VP of Engineering at IC Manage, "this becomes especially critical with globally dispersed teams working around the clock to meet tight deadlines".

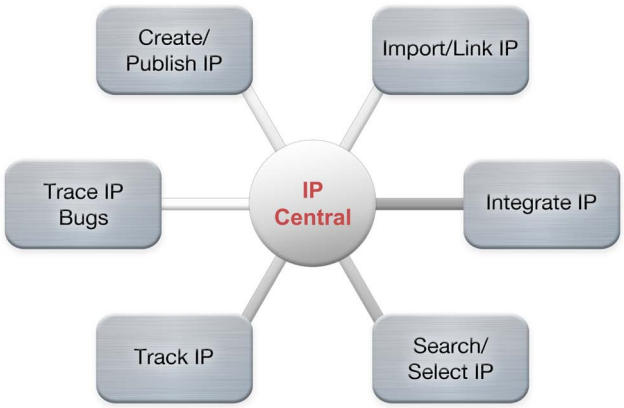
IC MANAGE IP CENTRAL -- MAXIMIZING IP REUSE

In 2011, after market success with its Global Design Platform (GDP) tools, IC Manage expanded GDP to include a comprehensive set of IP Reuse tools called IP Central. As shown in ***Figure 8***, IP Central offers designers the ability to rapidly publish and integrate IP, plus trace IP bugs dependencies, in their existing design flows. A strong benefit is that internal and third party IP can be imported or linked to IP Central from multiple commercial and open source data sources, as well as internal revision control systems.

What IP Central technology features offer is a "true fit rather than a best match" solution to design management. As noted by IC Manage, what's missing in most IP libraries today is an indication of the "state of IP, the grade of IP, verification, die field failures or the required voltage states." Apple's use of application processors and similar SOC designs for the iPhone, iPod and iPad illustrates an efficient reuse of IP across multiple generations of products. Application processors for the iPhone and the iPhone 3G used the same 90nm DRAM from Samsung. When the design was switched to the 65nm process, Apple stayed with its know partner Samsung and used similar technology for the iPod Touch and then the iPhone 3GS.

IP producers can use IP Central to more easily publish internal IP for reuse, using a checklist-driven flow with an encapsulated view of IP and IP properties. Managers can securely set IP usage permissions, and control use of selected IP. IP Consumers can search for IP according to complex specifications, view IP properties and status, and trace IP bug dependencies. Companies can then track where the IP is being used, which versions and by whom.

Figure 8: IC Manage IP Central Technology



IC Manage IP Central

Source: IC Manage, June 2011

Design and verification engineers spend about one-quarter of their time on design management tasks such as IP reuse, tracing bug dependencies, configuration management and version control. In published case studies by GN Resound and Foveon, IC Manage's Global Design Platform reduced design management time and accelerated IP reuse. An NVIDIA case study discussed IC Manage's high performance, scalability and derivative management functionality. IC Manage has proven that its Global Design Platform *(Figure 9)* with enhanced IP reuse can improve design team collaboration, and reduce designer time and project delays. By applying a suite of tools like those offered by IC Manage, designers not only minimize errors but also greatly improve their products' entire supply chain.

Figure 9: IC Manage Global Design Platform

Source: IC Manage, June 2011

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