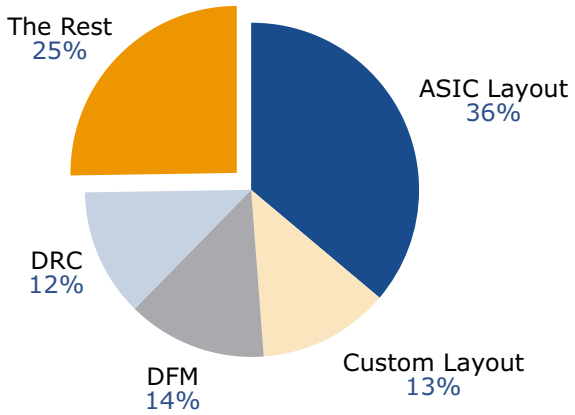
"EDA vendor Cadence Design Systems Inc. will eliminate 225 jobs—or about 5 percent of the company's workforce... Cadence said the job cuts will come primarily from resizing its worldwide field organization to current business levels, decreasing investment in the manufacturing side of design-for-manufacturing technology." EE Times
http://www.eetimes.com/news/design/showArticle.jhtml?articleID=217800664

ANALYSIS

There are two things. First is the 5% layoff. This is basically a sales layoff that we've been expecting for a few months now. That fact that is only 5%, way under some estimates, says that Cadence is recovering faster than expected.

Shutting down DFM is the other. On the surface it looks a good decision; they have little chance of catching up with Mentor or Synopsys. Look a little closer however and it brings up a problem with their long term strategy. Their biggest problem is with their back-end tools. DFM capability is becoming integrated with a majority of today's back-end tool set. At 65nm and below routers are all DFM capable. This is where Cadence has really been losing ground. Both Mentor and Synopsys have recently been successful in outsourcing some design tool research from semiconductor vendors; Mentor specifically in DFM. Without this leading-edge DFM knowledge, it will be highly improbable that Cadence can regain the technical lead in ASIC Layout, DRC and soon Custom Layout. Those three, plus the DFM tools, make up a majority of the IC CAD market dollars *(see Figure 1)*.

Figure 1: IC CAD 2007



(Source: Gary Smith EDA, June 2009)

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