GARYSMITH EDA
CONSULTING IN ELECTRONIC DESIGN

cadence™ + Mentor Graphics® ?

CADENCE'S HOSTILE TAKEOVER BID

One of the strangest comments in Cadence's somewhat surreal hostile takeover bid for Mentor was Mahesh Sanganeria's comment, "We do not believe the deal will face regulatory push back." With statements like that being thrown around we thought it was a good time to look at the actual numbers.

CADENCE + MENTOR COMPETITIVE POSITIONING

The mistake most financial analysts make is to look at EDA as one or at best three competitive environments. If you take time to download the three **EDA Wallcharts from our website** you will find that this is a market made up of 85 sub-applications as of the end of 2007, which comprise the competitive environments in EDA. There are technology adjacencies and marketing environments that allow you to combine these sub-applications to simplify your analysis but you need to have a background in all of these sub-applications to make intelligent combinations. A good example, and the simplest, is the Printed Circuit Board (PCB) market. PCB design tools are the oldest of the EDA tools. In the mid 1990's the acquisition of Cooper & Chan Technology (CCT), by Cadence, caused a 75% reduction in the number of PCB vendors. CCT sold the most popular PCB router of the time and once Cadence cut off licensing the router to other PCB vendors, most didn't have the R&D capability to develop their own router. At that point most Users started buying the bundled PCB tools offered by the three leading vendors. Therefore, we have been able to combine the 10 sub-applications that make up the PCB market, for this analysis. We've made some other combinations, such as Formal Analysis and Formal Verification, as they are adjacent technologies and we've dropped the sub-applications that have little impact on this competitive analysis, giving us 22 sub-applications that comprise the competitive landscape for a combined Cadence and Mentor company.

These numbers are their 2006 numbers as those are the most recent final numbers we have. The 2007 numbers are in; however they are not scrubbed - a six-week process that rigorously checks the inputs from our yearly market survey. We have compared the un-scrubbed 2007 numbers and in general it appears that Mentor has improved their competitive positioning while Cadence has remained flat.

TABLE 1: CADENCE/MENTOR 2006 NUMBERS - COMPETITIVE POSITIONING

	Cadence	Mentor	Other	Other %	Total Sub-Ap Mil $$$	Combined Mkt Share
ESL						
Architect's Workbench	in R&D	8%	Mathworks	92%	$38.0	8%
Algorthmic Synthesys	new tool	42%	Forte	28%	$20.9	42%
ESL Verification	95%	5%	none	—	$45.9	**100%**
RTL						
RTL Design	bunded	16%	Novas	45%	$97.3	16%
Mixed-Language Simulation	30%	35%	Synopsys	34%	$339.7	**65%**
Mixed-Signal Simulation	31%	53%	Synopsys	16%	$70.6	**84%**
Formal Analysis + Formal Verification	53%	13%	Synopsys	15%	$109.4	**66%**
RTL Synthesis	10%	6%	Synopsys	60%	$433.1	16%
DFT	15%	30%	Synopsys	22%	$99.2	45%
Design Team Acceleration & Emulation	63%	small	Eve	15%	$15.5	**63%**
Design Analysis	10%	small	Synopsys	87%	$70.5	10%
Analog Simulation	84%	small	Synopsys	13%	$86.2	**84%***
RF Design & Simulation	11%	none	Agilent EEsof	62%	$134.8	11%
Verification Team Acceleration & Emulation	73%	27%	none	—	$82.1	**100%**
Interoperability Tools	14%	small	Platform Computing	77%	$51.7	14%
IC CAD						
ASIC Place & Route	35%	1%	Synopsys & Magma	64%	$578.3	36%
Custom Layout	73%	9%	small players	18%	$210.0	**82%***
DRC	25%	60%	Synopsys	13%	$200.3	**85%**
Extraction	41%	17%	Synopsys	37%	$97.7	58%
Physical Analysis	43%	2%	Synopsys	19%	$107.5	45%
IC CAM (DFM)	6%	35%	Synopsys	55%	$225.4	40%
PCB						
Printed Circuit Board Design	24%	34%	Zuken (Japan)	10%	$505.4	**58%****

*** Comparable Tools Available**
**** Comparable Tools "Not" Available**
***** small indicates small % of market**

Area of concern
Possible trouble

Source: Gary Smith EDA - June 2008

The results aren't surprising. We found four areas of high concern and six that looked like trouble. In ESL there is a problem in the ESL Verification category. As ESL is the design level that includes both hardware and software design & verification, speed is of essence. The way that is accomplished in ESL Verification is with emulation. There are only three companies that have Emulation Boxes capable of functioning as an ESL Verification engine; Cadence, Mentor and Eve. A start-up Axis pioneered this category as an expansion to their Design Engineering Acceleration and Emulation (A&E) box. They were bought by Verisity who in turn was acquired by Cadence.

Next comes Mixed-Signal Simulation. Cadence has 31% of the market and Mentor has 53%, probably a little more than that in 2007. This gives the combination a 84% market share, well into the monopoly category.

Again, as in the ESL Verification, Verification Team A&E becomes a 100% market with the combination of Cadence and Mentor. The big problem is, that if Cadence is forced to divest one of the combination's two A&E groups, who are they going to sell it to ? A&E is the only hardware tools sold by EDA vendors, all the rest are software. Most EDA companies have avoided getting into the hardware business. You could say that Synopsys has already entered the hardware business with the purchase of Synplicity and their Hardi Rapid Prototyping system, but that is basically a board-based product and that's a long ways from a multi-million dollar A&E box that is housed in the "Glass House" and purchased as a capital expenditure.

The last one is DRC. Mentor is the market leader with 60% market share, and Cadence's legacy position of 25% drives their total market share into the danger zone.

If you look at the six that could cause trouble the first is Mixed-Language Simulation. This is pretty much a one-third, one-third, one-third market between Mentor, Synopsys and Cadence. Cadence has been slipping recently but their 30% market share and Mentor's 35% market share still puts them at 65%; a bit high for comfort.

If you combine Formal Analysis with Formal Verification, adjacent technologies, the combination of Cadence and Mentor gives them a market share of 66%. Again a bit high.

Design Team A&E really has only three fully capable vendors, Cadence, Mentor and EVE. Mentor has had a hard time getting into this important market but Cadence has done well with the Axis box. Eve is a new start-up who is doing well and the rest are Rapid Prototyping boards. Cadence holds a 63% market share; however if you remove the numbers for the Rapid Prototyping vendors, the numbers are a little grimmer; Cadence 81% and Eve 19%.

The next two are Analog Verification and Custom Layout. The combination of Cadence and Mentor would give market shares of 84% and 82% respectively. I have not red highlighted either as they both have to do with Cadence's long standing Analog Franchise. This franchise has recently come under attack by a group of start-ups, Ciranova being the main one, and now Magma and Synopsys. This year they will all announce tools that can read Pcells, the basic building blocks of Cadence's analog design system which are written in Skill, Cadence's proprietary scripting language which is the intellectual property that holds the franchise together. We therefore expect this competitive imbalance to sort it out in the near future.

The last is the Printed Circuit Board market as a whole. This is another special case. It's obviously trouble but when you dig into the market conditions it could easily be of high concern. The three main players hold 68% of the market with Zuken slipping behind the market leaders, Mentor and Cadence. The rest of the vendors, and there are quite a few, are either point tool vendors or vendors that target the lower price market. That means the smaller players, and even Zuken, would have a hard time filling the void made by a Cadence/Mentor merger. There would be no meaningful number two in the PCB market.

Now let's look at the numbers from a different angle and see if this merger makes any sense.

Table 2. Cadence/Mentor 2006 numbers – Leakage

TABLE 2: CADENCE/MENTOR 2006 NUMBERS - LEAKAGE

	Cadence	Mentor	Total Sub-Ap Mil $$$	Combined Mkt Share	Cadence	Mentor	50% Leakage
ESL							
Architect's Workbench	in R&D	8%	$38.0	8%	—	$3.0	$1.5
Algorithmic Synthesys	new tool	42%	$20.9	42%	—	$8.8	$4.4
ESL Verification	95%	5%	$45.9	**100%**	$43.6	$2.3	$1.1
RTL							
RTL Design	bunded	16%	$97.3	16%	—	$15.6	$7.8
Mixed-Language Simulation	30%	35%	$339.7	**65%**	$101.9	$118.9	$59.4
Mixed-Signal Simulation	31%	53%	$70.6	**84%**	$21.9	$37.4	$18.7
Formal Analysis							
+ Formal Verification	53%	13%	$109.4	**66%**	$58.0	$14.2	$7.1
RTL Synthesis	10%	6%	$433.1	16%	$43.3	$26.0	$13.0
DFT	15%	30%	$99.2	45%	$14.6	$29.7	$14.9
Design Team							
Acceleration & Emulation	63%	small	$15.5	**63%**	$9.8	—	—
Design Analysis	10%	small	$70.5	10%	$7.3	—	—
Analog Simulation	84%	small	$86.2	**84%***	$72.4	—	—
RF Design & Simulation	11%	none	$134.8	11%	$14.8	—	
Verification Team							
Acceleration & Emulation	73%	27%	$82.10	**100%**	$59.9	—	—
Interoperability Tools	14%	small	$51.7	14%	$7.2	—	—
IC CAD							
ASIC Place & Route	35%	1%	$578.3	36%	$202.4	$5.8	$2.9
Custom Layout	73%	9%	$210.0	**82%***	$153.3	$18.9	$9.5
DRC	25%	60%	$200.3	**85%**	$50.1	$120.2	$60.1
Extraction	41%	17%	$97.7	58%	$40.1	$16.6	$8.3
Physical Analysis	43%	2%	$107.5	45%	$46.2	$2.2	$1.1
IC CAM (DFM)	6%	35%	$225.4	40%	$12.5	$78.3	$39.2
PCB							
Printed Circuit Board Design	24%	34%	$505.4	**58%****	$121.3	$170.3	$85.2
OTHER					$268.4	$60.4	$30.2
TOTAL					$1,349.0	$728.5	$364.3

*** Comparable Tools Available**
**** Comparable Tools "Not" Available**
***** small indicates small % of market**

Area of concern
Possible trouble

Source: Gary Smith EDA - June 2008

It's been interesting to watch the reasons for this merger change from the supposed synergies between the two to what now Wallstreet calls Leveraging Up, a term that should strike fear into most Cadence Employees. The idea is that a company with larger financial resources, and an aging product line, acquires a company with smaller financial resources and a more attractive product line,

throws away their old products and reinvents itself as a leading-edge provider of whatever product is involved. The question that never gets asked, by Wallstreet, is why was the original product no longer state of the art ?

What invariably happens is called Leakage. That term describes the number of customers, and related revenue, that decide to jump ship and move to a competitor. During Hostile takeovers that can be quite high. The loyalty is with the company being bought, after all there were reasons beyond product that they were not buying from the acquiring company. In the short term you need to take into consideration the chaos in the sales organization this type of merger produces, leaving openings for the competition to take orders away from the combination. And long term there is the loss of R&D resources both by engineers that do not want to work for the hostile acquirer and through the inevitablele layoffs this much product overlap creates.

At 50% leakage, which is certainly possible between the hostile takeover, regulatory mandates and Cadences already declining market share, Cadence would end up with an extra $364 million in revenue. At 30% leakage that number would be $510 million, so you have a three or four year payback on the $1.6 billion dollars spent.

Another strange comment coming out of Wallstreet is the possibility of Synopsys becoming a white knight. I guess they don't hear all of the laughter coming out of Mountain View right now. If the merger goes through Synopsys will pick up $200 to $300 million dollars from the leakage, plus some of Mentor's top people. Not bad for doing nothing. Plus Synopsys realizes that a Synopsys/ Mentor merger makes as little sense as a Cadence/Mentor merger. Not that they wouldn't love to have the Calibre product line, but that would get into regulatory problems on the DFM end.

THE OUTCOME

We can imagine three possible outcomes. The first that came to mind was the implosion of Daisy in 1989. The environment was the same. Daisy had been replaced as the number one EDA vendor by Mentor. They had lost the technical lead and were declining in revenue. They needed a merger to bring them out of their downward spiral. However when you look into the bankruptcy, it was their irresponsible borrowing in order to pull off the merger that did them in. Cadence is in much better financial shape.

The horror story from the design community is this. 1. The merger goes through. 2. Through the chaos there is a considerable loss of R&D engineers. 3. To further the problem Cadence under invests in R&D. 4. And the combine companies end up missing the window for the 32/22nm tools. This would be strike three for Cadence and they would no longer be considered a viable EDA supplier to the Power Users, the largest market in EDA. That would leave Synopsys, and in the back end Magma, as the only viable major EDA vendors. This could drive the semiconductor community into reverting to in-house tool development to solve their design problems.

The most probable outcomes come from the Semiconductor Industry. In the late 1980s GE acquired RCA semiconductor, both were roughly $400 million operations. Then Harris semiconductor, another roughly $400 million company bought the combined RCA and GE Semiconductor operations. When the dust settled, Harris emerged as a roughly $400 million company.

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