WELCOME TO 22 NM DESIGN – IT AIN'T GOING TO BE EASY

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The transition from 32 nm to 22 nm silicon will have a major impact on the design community. The most obvious is the increase in process variation. This affects timing but more importantly it affects power. Because of this we are seeing a dramatic increase in the 22 nm process design rules. In turn you will see more and more design teams deciding to leave the IC Layout portion of the design to the experts.

The effects of 22 nm on the EDA vendors will be a combination of opportunity and shrinking IC Layout seat count. Although the new design rules moving toward structured silicon reduces the need for OPC (Optical Correction) tools, the move to double patterning gives the OPC tools new challenges, resulting in overall market growth. The variation problems will also drive the demand for DFY (Design for Yield) tools. The new variation challenges require the IC Place and Route tools take an active part in insuring the robustness of the final layout, therefore growing the IC Layout market for those tools that keep up with the 22 nm challenge.
This shift in responsibility won't give the circuit designers a free ride. They have more than enough to do to keep the power problem under control. For all the work we've done in decreasing power at the IC CAD level, we need to address the eighty percent of the power problem that is introduced during the design process.

22 nm puts over two billion gates at the design engineer's disposal. There are a lot of reasons why they aren't using that many; cost is one, design time is another, but the main one is power. One of the ways a designer can get around the power problem is to simply turn off unused portions of the circuit. This Dark Silicon is growing as these designs get larger. The technique is especially useful in application's driven designs such as cell phones. You can only do so many things at a time, on a cell phone, yet the users are demanding more and more functions be made available in the next generation smart phones.

The one tradeoff microprocessor vendors don't like to talk about is frequency. An engineer has three things he can play with. He can vary the size of the design, the power (or energy) used by the design, and the frequency. In the mobile community the problem isn't power, the power envelope is a requirement. That leaves the gate count and the frequency as the two variables. The average high end mobile design only uses about twenty percent of the available silicon. In an app driven world the pressure will be to use more gates. If something has to move it must be frequency, and it has to move down. Even today's cell phone designers laugh at the microprocessor vendors that brag about their multi-GHz processors. What they really want is a processor architecture that will allow them to operate multiple applications at 300 MHz's.

So welcome to the world of 22 nm design. It should be fun.

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