DVCON 2012 TAKES ON THE SYSTEM LEVEL VERIFICATION CHALLENGE

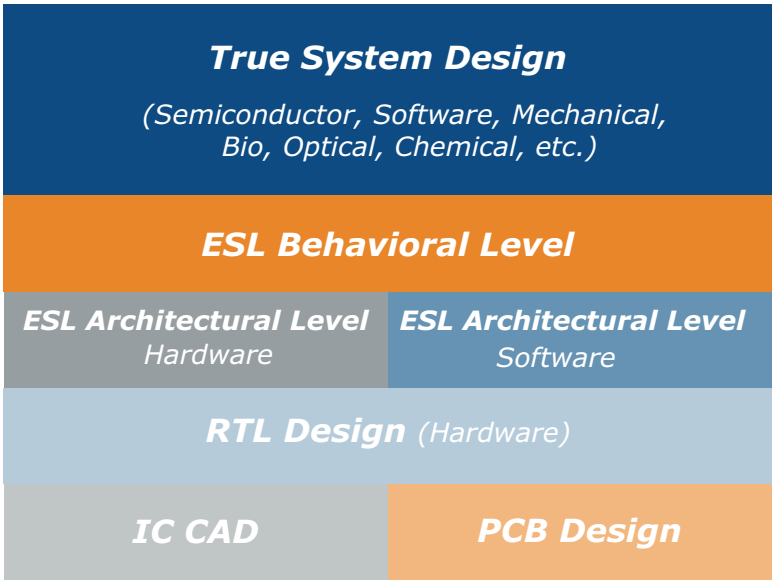
DVCon continues to grow as a conference, both in importance and in quality. DVCon 2011 was a major step forward in the quality of their technical content. DVCon 2012 continued this trend while stressing the importance of verification in today's design world. As one speaker noted verification engineers are no longer the design engineers that were demoted after failing a design task.

DVCon 2012 takes on the System Level Challenge

This wasn't a conference of major breakthroughs. This was a show of the standardization and consolidation, of the various RTL verification flows and the move upwards to the ESL Verification flows. This is where it broke down. There was a lot of skepticism in the audience around the use of UVM in the System Verification flows. One comment was that random verification techniques in a design space as large as a system would be so time consuming that it would be useless.

If DVCon did nothing else it got the verification community thinking about the system level problem. I believe the attempt to move our verification methodologies up into the ESL Architectural level will fail. ESL Behavioral Level is where verification should start. That will cause us to completely rethink our verification approach. You can't solve a system level problem by borrowing techniques from the RT Level flow. I believe DVCon 2012 will be seen as the point where we went back to the drawing board on System Level verification.

Design Hierarchy



GARY SMITH
PHONE +1 (408) 985-2929
FAX +1 (408) 985-6611
gary@garysmithEDA.com