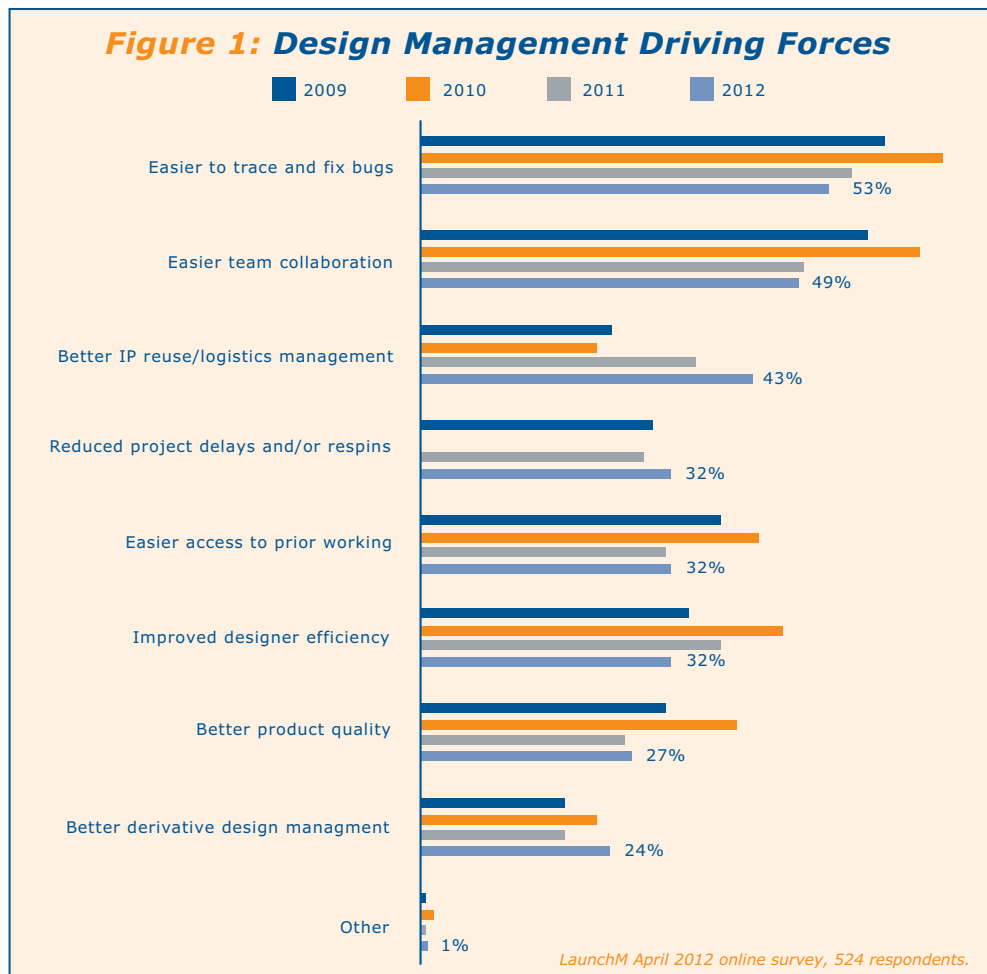


The 2012 Design & IP management survey of 524 designers and managers came up with a few surprises this year. As far as the shift from internal or open source software, to commercial Design Data Management software is concerned the study reaffirmed previous studies. With the average high-end mobile design coming in at 134 million gates the design files are requiring sophisticated Design Management software that has been specifically targeted toward IC Design. General purpose or PDM tools don't solve the problem.

DESIGN DATA MANAGEMENT AND IP REUSE

Design Management Driving Forces

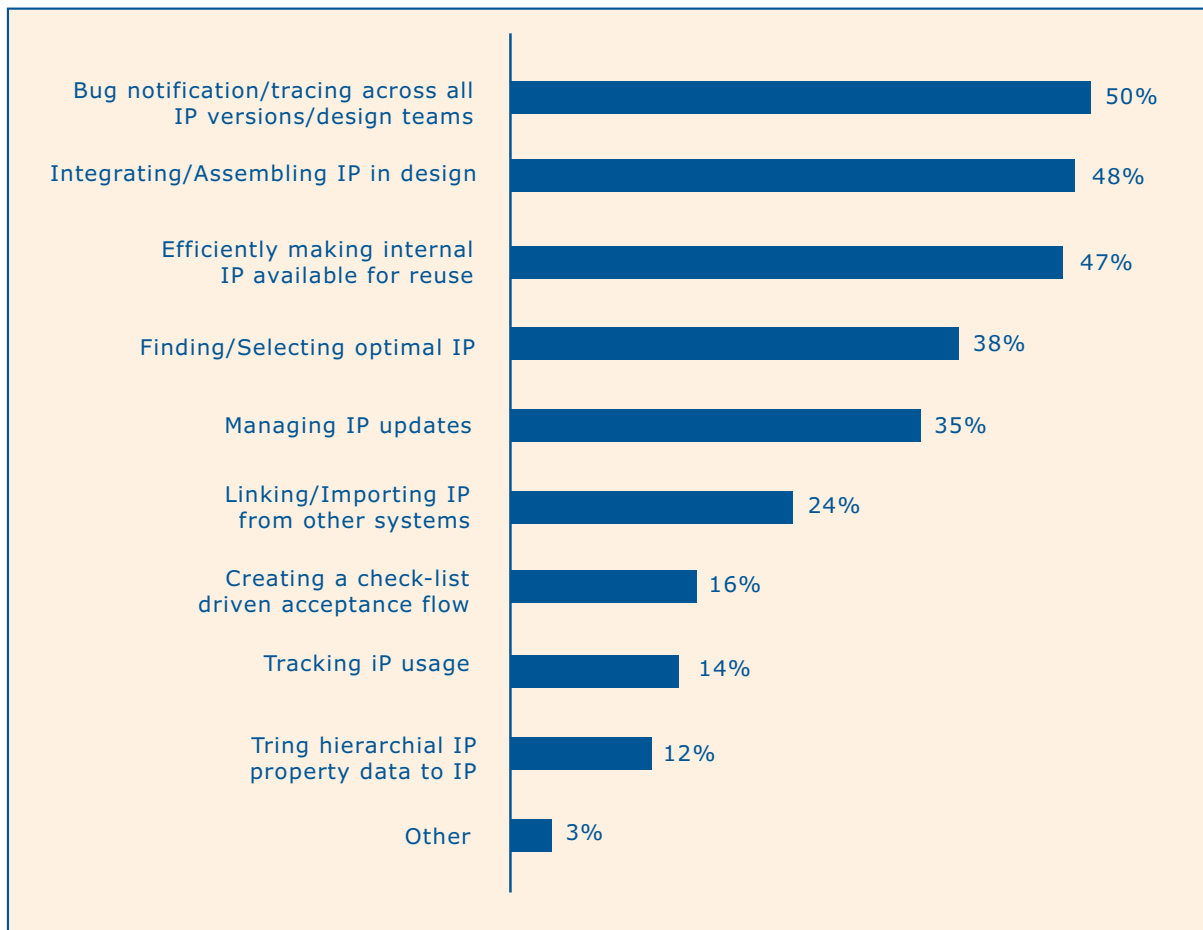
The surprise this year was the emphasis on Bug tracking. As I said in my What to See @ DAC talk a few weeks ago, this was the year of Debug. We are debugging everything: hardware debug, software debug, test-bench debug, power debug, you name it and debugging it has become a major problem. Along with that this survey shows that tracking your debugging process has become one of the top concerns of the design community. With the new emphasis on Platform IP the number three concern is better IP management (see Figure 1).



IP MANAGEMENT CRITICAL FEATURES

Again Bug management hits the top of the list with the next two places featuring IP assembly and the use of Internal IP, increasingly important in the new world of Multi-Platform Based design (see Figure 2).

Figure 2: IP Reuse Management Critical Features



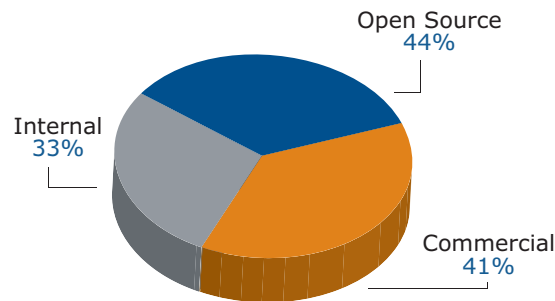
LaunchM April 2012 online survey

DESIGN MANAGEMENT ADOPTION TREND

As stated before, General Purpose tools aren't solving the problem. This shift to commercial tools grew market share by 17% annual growth for each of the last two years. Also 63% of designers are now using Design Management software (see Figure 3).

Figure 3: Design Management Adoption Trend

In 2012 63% of organizations used a DM System. Of those using a DM system, 41% used a commercial system. Only 30% of the respondents, that used DM systems in 2010, used a commercial system.

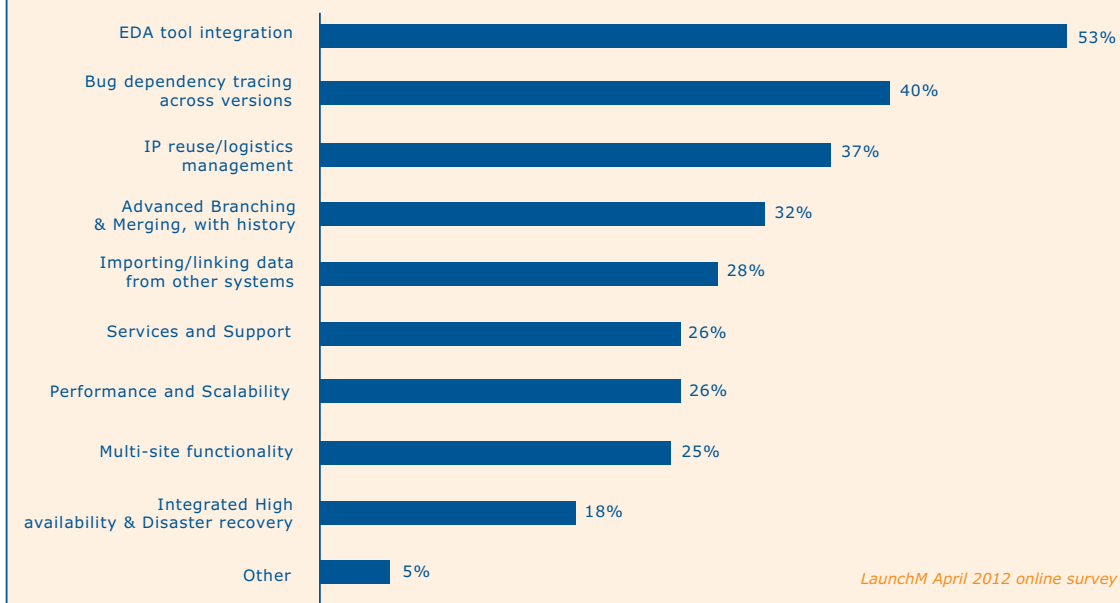


LaunchM April 2012 survey

OPEN SOURCE DESIGN MANAGEMENT HOLES

Any CAD team can tell you that one of their top problems is integrating software with their commercial EDA tools, so it's not surprising that EDA tool integration is the number one "hole" in open source design management tools. Again bug tracing is another major problem, followed by IP management (see Figure 4).

Figure 4: Open Source Design Management Missing Functionality

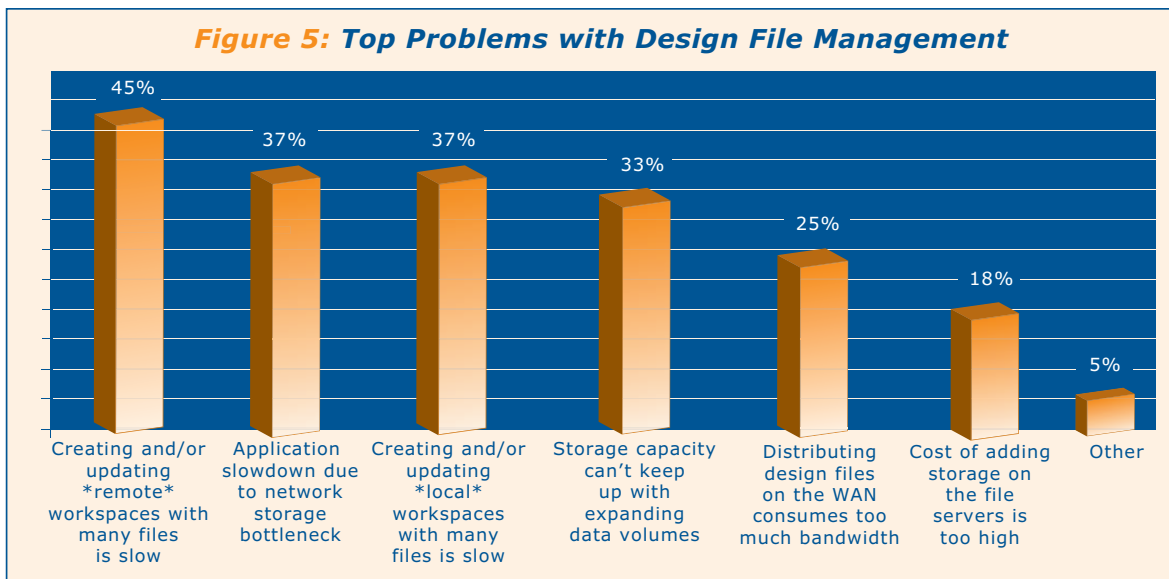


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NETWORK STORAGE BOTTLENECKS

Design File Management Top Problems

When you have 134 million gates you have very large files. These files eat up a lot of storage space and they take a lot of time to download. Software not designed for the IC design task becomes very frustrating to use, especially with IT breathing down your neck for taking up most of their storage capacity. Commercial EDA design management software's major advantage is the tricks they've learned to minimize your frustration (see Figure 5).

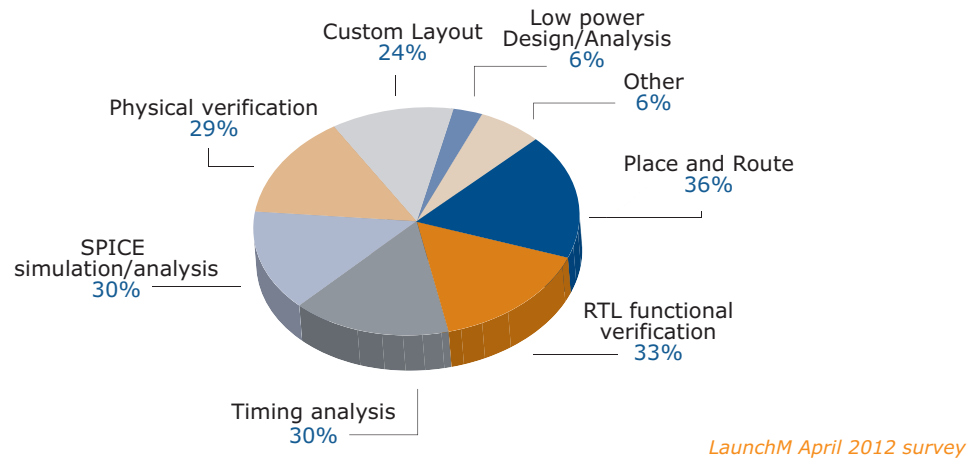


LaunchM April 2012 survey

EDA TOOL SLOWDOWN

Another frustration is the EDA tool performance. The survey showed a 30% slowdown in iteration time due to network storage bottlenecks. If you're running your tool locally the tool runs fine (or at least to specification). Once you run it remotely from your Computer Farm, it's a dog. What happened: Network Bottlenecks (see Figure 6).

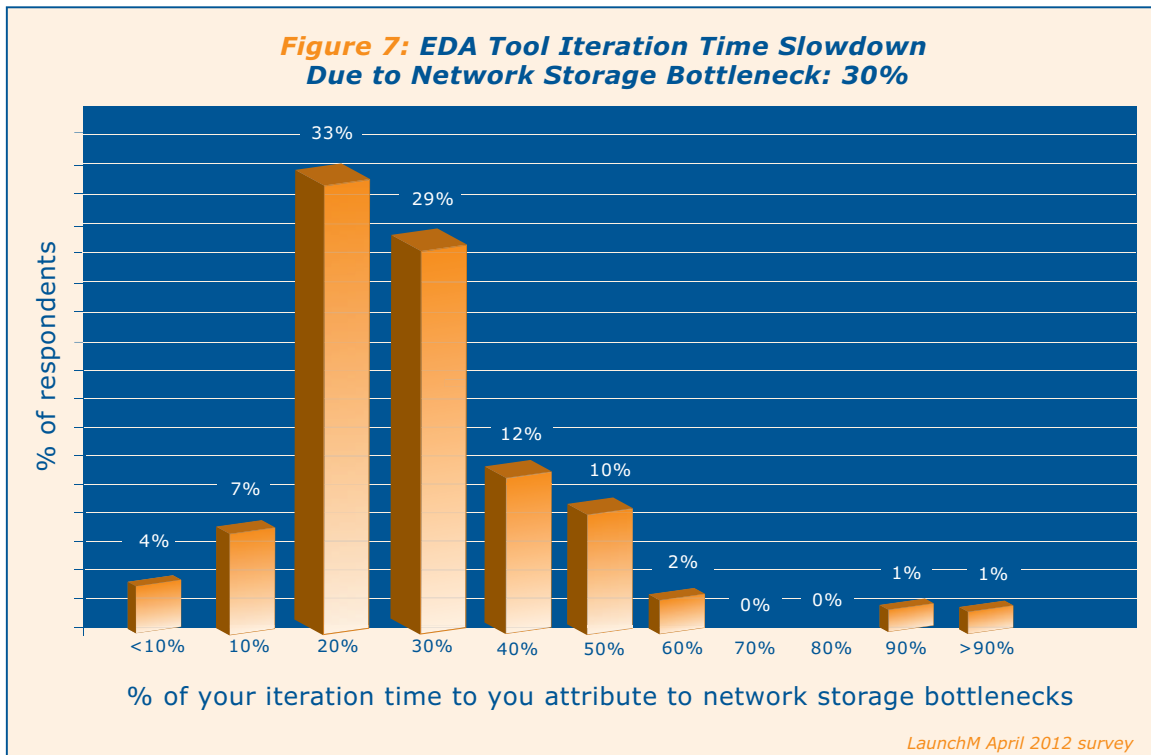
Figure 6: Applications with Slowdown due to Network Storage Bottlenecks



TOP ISSUES WITH SYMBOLIC LINKS FOR DISK SPACE MANAGEMENT

Disk Space Management is in a world of its own. The problems of mirrors, version control and storage management are not something a design engineer wants to be concerned with. This is where Design Automation should be doing its part. That is what EDA is all about isn't it? (see Figure 7).

Figure 7: EDA Tool Iteration Time Slowdown Due to Network Storage Bottleneck: 30%



IN CONCLUSION

So if you're not part of the 26% - (41% of 63%) of the companies using commercial EDA Design Management, I don't want your job. I have enough headaches design 134 million gates as it is. Oh, and if you don't support Windows I don't care either.

DESIGN MANAGEMENT AND IP REUSE BEST PRACTICES PANEL AT DAC 2012

I participated on a DM-IP reuse panel at DAC 2012, where AMD, NVIDIA and Broadcom discussed the best practices they use for Design Management and IP reuse, utilizing IC Manage's DM system. The key takeaways I got from it were:

- 1) Nvidia's "If it isn't checked in, it doesn't exist."
- 2) Broadcom's "Bug tracking is key."
- 3) AMD's "Insuring US Export Control Compliance."

From IC Manage

IC Manage provides high performance design and IP management solutions for use with existing full-custom, mixed-signal and digital design flows. Per Dean Drako, IC Manage's President and CEO, the company's focus is to improve semiconductor company engineering ROI and accelerate their market delivery across the enterprise. According to Drako, "People spend a quarter of their time on design management related issues. The key is to make them more effective through real-time design collaboration, while improving IP reuse and bug management across the enterprise."

IC Manage is continuing their expansion into large enterprise accounts. As mentioned above, three of IC Manage's customers AMD, NVIDIA and Broadcom, discussed their Design Management and IP reuse practices utilizing IC Manage's DM products at DAC 2012. Additionally, Altera recently moved to using IC Manage GDP and IP Central, and a Broadcom case study was recently released. Broadcom discussed adopting IC Manage after an evaluation by three different groups. The case study covered IC Manage's Global Design, IP Central, and IC Manage Views. Broadcom emphasized bug dependency tracing, creating virtual copies instead of physical copies, security, and network storage acceleration.

IC Manage Global Design Platform

IC Manage GDP design management system supports multi-site collaboration of SoC, IC and FPGA development teams. GDP allows them to dynamically manage design data through tapeouts. GDP manages revisions of all data types, including binary data, RTL, software, and EDA databases. It is built on Perforce, an industry standard SCM, to give hardware and software developers a unified development model for all data types.

GDP uses virtual referencing techniques instead of creating physical copies of different IP/design modules in multiple repositories. The design module/IP is cloned to create virtual copies through pointers, maintaining the relationships so that each IP version can be separately and independently tracked in real-time across the enterprise.

Design teams and management can track and view which IP/design modules different designers have checked out. It offers branching and merging with the full project history of files or data types, and bi-directional updates between the original IP and its derivatives.

As noted by Shiv Sikand, VP of Engineering at IC Manage, "The key with virtual copies is that you can understand where everything went. So if I reused a block in 6 different chips, I have a record where I can simply get a report, and know exactly where it went."

IC Manage IP Central

Broadcom and Altera have deployed IP Central, which IC Manage announced at DAC 2011. IP Central offers enterprise-wide bug dependency tracing and bug fix propagation. It integrates its IP repository with bug tracking systems such as JIRA and Bugzilla.

All identified bugs and bug fixes associated with each IP block are automatically recorded in both the bug tracking system and the IP repository. Design and verification teams can view and trace the bug history for every IP they work with across all versions and designs and can be automatically notified for new bugs and propagate fixes. IP data can also be imported or linked from multiple commercial and open source design management systems and internal databases and file systems to create a central view of IP assets.

IC Manage encapsulates all relevant property data associated with each IP element into the IP repository, such as design data, bug status, assertions, constraints, timing goal status, margins, power consumption, electrical data, regressive results, and documentation. Design team members involved can mark or flag IP status as the development and verification process progresses, i.e. checklist-driven design.

IC Manage Views

In 2012, the company announced IC Manage Views storage acceleration software, with a goal to remove network storage bottlenecks. IC Manage Views is a version aware, virtual file system that presents complete workspace views, while transferring data on demand to a local file cache. By removing network transfer bottlenecks in this manner, it accelerates EDA tool performance, achieves near real-time workspace syncs, and reduces storage utilization. Per IC Manage, a one gigabyte, 10,000 file workspace takes approximately one second to populate using IC Manage Views, allowing tools to run immediately.

IC Manage Views utilizes local storage for reads to achieve faster EDA tool performance - design engineers get local speeds and avoid delays caused by network latency. Views also uses network storage for writes to provides consistent data storage and access. As noted by Drako, "using virtual file distribution gives you the ability to accelerate your EDA tools to eliminate bottlenecks, while maintaining workspace control and stability."

As discussed earlier in this report, the cost of storage capacity needed to keep up with expanding design data is extremely high. IC Manage Views substantially reduces storage requirements by automatically rotating least recently used files to stay within workspace cache quotas, and handles cache recovery in the event of failures or errors. It is compatible with all storage technologies and works at both local and remote sites.