IN SEARCH OF A POWER MODEL

Last April, at **EDP 2011**, I began a search for a power model. Power models existed but they were for high performance, GHz-based designs. I was unable to find one for a low power, mobile SoC. The search ended up being one of the most difficult I have undertaken in my eighteen years as an analyst. The final model was put together on January 21st, a full nine months after I started.

The results were interesting. I will say that this was a US only survey; adding Asian and European data may change the results, but probably not by much. Especially since the SoC criteria was that it was an average high-end SoC designed for a mobile application. Most inputs were from cell phone designers. Here are some of the inputs.

1. Power budgets were 5 watts for a low end phone and 8 watts for a high end phone.
2. Because of the power constraints they all projected using less than 25% of the available gates for the foreseeable future.
3. Because of the power constraints low end phones were operated at an average frequency of 400 MHz; high end phones operated at an average frequency of 800 MHz. The maximum frequency was 1.2 GHz or less.

The good news was that they came up with a wish list of tools and methodology improvements that should allow us to increase one of the **three main variables: power, gate count, or average frequency.** With the constant demand for more applications my bet is that engineers will choose gate count.

The wish list average frequency was 300 MHz; of course that's with no degradation of performance. One of the ways to do this is the increased use of Dark Silicon. Having a good percentage of your design operating at 0 MHz, a high percentage of the time, really helps keep down your average frequency. Another interesting idea is what I call Speed Bursting. Since power isn't the real issue, it's energy consumption; sometimes you can ramp the speed of you processor into the GHz range, and complete a task using less energy than you would at you average MHz frequency.

One methodology that is getting a lot of attention recently is TSV (Through Silicon VIAs). Minimizing the path between your processor and you memory really saves energy consumption (i.e. power). That could become the main driver for the 3D technology.

In April I **chaired a session** on low power design at **EDP 2012**, and gave a talk, with the complete results of Power Model Search, at EDP 2012. There was also another session on 3D ICs that had some good power information. Check out the EDP website for **my presentation**.

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