GARYSMITH EDA
CONSULTING IN ELECTRONIC DESIGN

RTL Market Trends 2017
The Changing Face of RTL

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EXECUTIVE SUMMARY

It's quite a relief that electronic system level (**ESL**) growth in 2016 returned to a healthy double-digit range. The prior year brought a measly 1.5 percent growth for the ESL market, far from the level desired for an up-and-coming, next-generation set of design tools. In fact, the aberration in 2015 was primarily due to a difficult year for a single vendor (Mentor Graphics) in the ESL space, not a market-wide phenomenon. The proof that this was merely a temporary blip is borne out in looking at how 2016 growth jumped back, reassuring the industry that ESL tools aren't just a shortlived novelty. Though still not used by every design team for every project, ESL tools are certainly developing traction in the marketplace and gaining acceptance as beneficial to the design flow. We continue to anticipate robust growth for ESL in the coming years.

The register transfer level (**RTL**) tools market turned in very respectable growth in 2016. Starting with our 2014 market data, we added a new sub-application in RTL – intellectual property (IP), which significantly increases the overall size of the RTL market by about one-third. Over the past six years, the RTL-and-Below market has been continually growing, though always in the single digits. On the surface, it looks like users have continued to put steady investment into RTL and gate-level tools for the past six years, but no more than that. However, once we peel back the layers, we see that there are definitely opportunities for growth in RTL. As always, users are facing increasing time-to-market pressures but are reluctant to invest heavily in new tools and software if they can make do with the old. Designers don't have to take the time to learn new software if they are productive enough already. Meanwhile, design size and complexity are increasing, and designers need ways to handle this complexity.

The **IC CAD** market had another year of very solid growth, too. The boundaries between the traditional steps of a physical design flow – placement, CTS, routing, post-route optimization – are breaking down, and designing for routability and timing closure becomes necessary as early as the power grid creation stage. This calls for different design flows than what exists today. Power integrity optimization needs to be taken in as a proactive step at the floorplanning/power grid stage instead of a reactive step later in the backend process. Shifting to 10nm and 7nm (for 2020 production) means a need to work closely together in multidiscipline approaches and crossing the boundaries of traditional design flow steps, in order to allow for design convergence and timing closure. It also

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means that over-the-wall delivery (e.g. from a team in the US to another in India, for instance) is very challenging and will put stress on some of the existing organization structures built around the traditional flow.

In 2016, positive growth returned for printed circuit board (**PCB**) tools. The challenges facing many PCB engineers are to develop high precision CAM tooling, advanced data integrity tools and next generation power tools. PCB engineers have found total allotted design cycle time decreased, especially as incredibly complex chip processes, new materials, advanced package designs and board level connectivity advanced from research to reality. Design flow errors, waste and product recalls, re-work and extra prototypes increased and costs exceeded original budgets. Adding layers of complexity requires different layers of integration and increases power supplies and power consumption. The "next generation" of products requires new solutions that reduce wiring, coding, time to market, cost and improve efficiency.

Slicing and Dicing Market Statistics Data

Like so many technology industries, EDA is perpetually facing new technical and business challenges. Between progressing to an era of System Level Design and contending with the world of Internet of Things (IoT) designs, we need to look at the market, and therefore the numbers, from other perspectives. Design methodologies and business requirements are often developed within vertical industry markets. There is no single, overarching systems market for all types of end products; fighter jets and cell phone have vastly different design challenges, after all. Therefore, it makes sense to present Market Trends data in an alternate way also, to correspond to this vertical industry approach.

These types of second-cut data reports are usually created on an on-demand basis. With frequent demand, though, a second-cut report may become standard report. As the system level design methodology begins to take shape, we may extend our reporting into multiple industry reports, depending on demand.

INTRODUCTION

The "RTL and Below" market turned in decent growth in 2016, growing over 6 percent to reach $4792 million in 2016. Readers should note that this figure is much greater than what we have historically reported. Starting in 2014, we added a new sub-application in RTL – intellectual property (IP), which significantly increases the overall size of the RTL market by about one-third. Over the past six years, the RTL and Below market has grown, albeit always in the single digits. On the surface, it looks like users have continued to put steady investment into RTL and gate-level tools for the past six years, but no more than that. However, once we peel back the layers, we see that there are definitely opportunities for growth in RTL.

OVERVIEW

This report comprises the "RTL and Below" section of the EDA 2017 Market Trends. "RTL and Below" includes RTL (register transfer logic), gate level and transistor level design tools. These tools, along with ESL (electronic system level) tools, make up the CAE market for EDA tools. In this report we will discuss market share, trends, and forecasts for key "RTL and Below" sub-applications that have the most impact on the overall EDA landscape.

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$3,000

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